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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/488,942	01/21/2000	Paul W. Sherer	09764-003531US	5139

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EXAMINER	
DINH, DUNG C	
ART UNIT	**PAPER NUMBER**
2153	

DATE MAILED: 03/01/2004

8

Please find below and/or attached an Office communication concerning this application or proceeding.

4

Office Action Summary	Application No.	Applicant(s)	
	09/488,942	SHERER ET AL.	
	Examiner	Art Unit	
	Dung Dinh	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 18-28 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 18-28 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claims 18-21, 22, 26, and 27 are rejected under 35 U.S.C. § 103(a) as being unpatentable over AMD's Am79C830 FORMAC Plus as disclosed in "The SUPERNET 2 family for FDDI - 1991/1992 World Network Data Book" (the publication). Prior art submitted by applicant in parent application file 09/028,088.

As per claim 18, the publication discloses a communication adapter with transceiver having transmit buffer, receive buffer, and control circuitry [figure on page 2-4]. The publication discloses readout of a frame while it is being received to reduces delay in waiting for a complete frame [page 2-37, col.1 "Threshold Detection" paragraph]. The publication discloses interrupt circuitry [page 2-36, col.2 "Node Processor (NP) Interface"]. The publication discloses early receive interrupt once a predetermined number of bytes [threshold] of data packet less than all of said

data packet has been received [Apparent from page 2-32 col.1 "INNTERRUPTS. The interrupt signals MINTR1 or MINTR2 ... are asserted when FORMAC Plus status changes", page 2-52 col.2 "The receive frames are loaded into the buffer memory ... for single-frame receive mode ... The RDATA timing depends upon the receive threshold value...", page 2-64 bottom of col.1 "the ST2 register contains status bit that may generate maskable interrupts on the MINTR2 pin", bottom of col.2 "Receive Frame. RSCVRM (bit10) - This bit is set, during single-frame receive-mode operation, to interrupt the NP and indicate that data is present in the buffer memory"].

The document does not teach Ethernet control circuitry and host adapter interface. The Ethernet control circuitry and host interface are well known to one of ordinary skill in the art of network adapter design. The specific type of network use (Ethernet vs. FDDI) would have been a design choice and an obvious variation from the teaching of the document. It would have been obvious for one of ordinary skill in the art to adapt the teaching of the document to an Ethernet network adapter because it would have provide more efficient processing of Ethernet data packets.

As per claim 19, The AM79C830 is contained in a single application specific integrated circuit (ASIC). The publication does not specifically teach Ethernet control circuitry. However,

it would have obvious for one of ordinary skill in the art to apply the early interrupt to a Ethernet control circuitry because it would have reduces delay in waiting for a complete Ethernet frame.

As per claim 20, The publication discloses the threshold is programmable [page 2-97 "Frame Threshold Register. FRMTHR"].

As per claim 21, the publication discloses the circuit is programmable to generating a packet transmit signal when the buffer contains a predetermined number of bytes [page 2-98 col.1 "Transmit Threshold. XTHR"].

As per claims 22, the publication discloses method of tranferring a packet of data comprising the steps of:

a) receiving from the cummunication media and storing in a receive buffer a first threshold number of bytes of the packet [page 2-37, col.1 "Threshold Detection"];

b) thereupon generating a first early interrupt from the adapter to the host computer [apparent from page 2-52 col.2 "The receive frames are loaded into the buffer memory ... for single-frame receive mode ... The RDATA timing depends upon the receive threshold value..."; page 2-64 bottom of col.1 "the ST2 register contains status bit that may generate maskable interrupts on the MINTR2 pin"; bottom of col.2 "Receive Frame. RSCVRM (bit10) - This bit is set, during single-frame receive-mode operation, to

interrupt the NP and indicate that data is present in the buffer memory"];

c) thereafter receiving from the communication media and storing in the receive buffer a remainder of the packet [page 2-37, col.1 "Threshold Detection" - "...read out of the frame can then take place at the same time that the frame is being written"].

The publication does not specifically disclose the host employing a software driver allowing for early indication. It is well known in the art to employ software driver to communication to media adapter. It is inherent that a system having an adapater using the AM79C830 chip would have a driver for interface the adapter to the host. It would have been obvious for one of ordinary skill in the art to have the software driver allowing for early indication because it would have enabled the system to make full use of the AM79C830 capability.

As per claim 26 and 27, it is rejected under similar rationale as for claim 22 above. The publication discloses the early threshold is applicable to both transmit and receive mode [see page 2-37 col.1 "Threshold Detection" paragraph].

Claim 23 is rejected under 35 U.S.C. § 103(a) as being unpatentable over the Am79C830 publication and further in view of Firoozman US patent 5,210,749.

As per claim 23, the publication does not disclose determining the threshold value based on the latency of the host computer and the network. In similar field of invention, Firoozman teaches determining the threshold value based on the latency of the host computer and the network (col.14 lines 55-64). It would have been obvious for one of ordinary skill in the art to use Firoozman teaching with the Am79C830 publication because Firoozman teaches an improvement on the application of the Am79C830 chip.

Claim 24, 25, and 28 are rejected under 35 U.S.C. § 103 as being unpatentable over the Am79C830 publication and Firoozman US patent 5,210,749 and further in view of Bentley et al. patent 4,860,193.

As per claim 24, the publication and Firoozman do not specifically teach adjusting the threshold. In similar field of invention, Bentley teaches adjusting the buffer threshold according to previous data block length to better adapt the buffer to the data length so as to reduce latency. Therefore, it would have been obvious for one of ordinary skill in the art to adjust

the threshold value so as to maximize throughput and reduce latency.

As per claims 25 and 28, they are rejected under similar rationale as for claim 24 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung Dinh whose telephone number is (703) 305-9655. The examiner can normally be reached on Monday-Thursday from 7:00 AM - 4:30 PM. The examiner can also be reached on alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenton Burgess can be reached at (703) 305-4792.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2100 Customer Service whose telephone number is (703) 306-5631.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, DC 20231

or faxed to: (703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA, Fourth Floor (Receptionist).

Dung Dinh
Primary Examiner
February 26, 2004